CFET - A New High Quality MMIC Control Device

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Abstract

A new gallium arsenide (GaAs) device developed for use in microwave monolithic control circuitry has been demonstrated. Known as a CFET, for Control Field Effect Transistor, this device eliminates the need for a conventional submicron gate by achieving control by use of a gate located behind the source-drain channel. The resulting capacitance is smaller than a conventional MESFET, resulting in a figure of merit of 800 GHz as compared to 250 GHz for a conventional MESFET. The device capabilities are demonstrated by measured performance of a SPDT switch providing 0.35-dB insertion loss and 20-dB isolation over the dc -10.0-GHz frequency band.

Introduction

In most microwave radars, signal processing is required to achieve high performance in today's hostile and unpredictable environments. As illustrated in the block diagram of Figure 1, these control systems liberally use control elements for functions such as switches, attenuators, phase shifters, and limiters. Improved control element performance has been achieved through the use of a new device known as the CFET, for Control Field Effect Transistor, that eliminates the need for a conventional submicron gate by use of a gate control element located under the source-drain channel. Device capacitance is smaller than that of a conventional MESFET, resulting in a high figure of merit of 800 GHz. Use of this device in wideband transmit/receive (T/R) modules enhances the receiver noise figure and third-order intercept (TOI) performance, resulting in greater dynamic range.

Description

To improve the figure of merit for a control device, the on-resistance and/or off-capacitance must be reduced. The CFET device, shown in cross section in Figure 2, achieves both of these improvements by removing the gate from the conventional position on top of the channel and placing it beneath the channel. This eliminates the depletion capacitance that exists under the gate of a typical MESFET and permits the source-drain contacts to be moved closer together, resulting in lower resistance. The CFET process begins with an epitaxially grown structure shown in Figure 3. The n- and p-layer doping and thickness are carefully controlled so that full depletion of both layers is achieved at pinchoff. The first step in processing is formation of the Au/Ge ohmic contacts, which is the same as for MESFETs. The ohmic contacts,

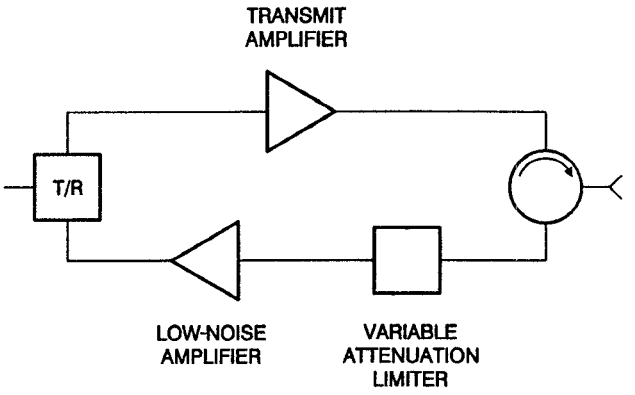

Figure 1. System Block Diagram

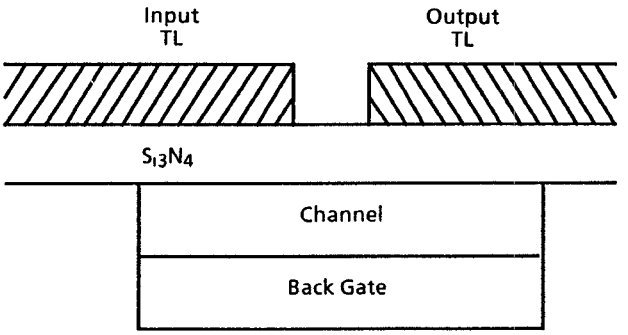

Figure 2. CFET Cross Section

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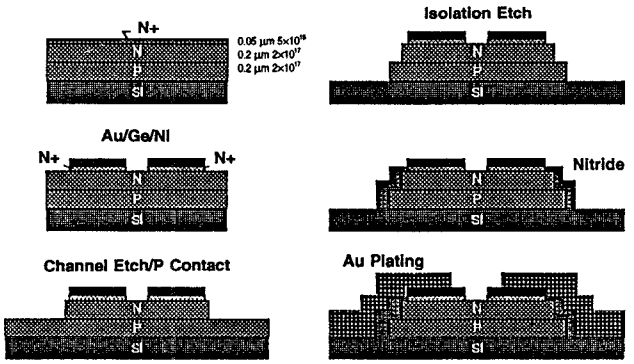

Figure 3. CFET Process Flow

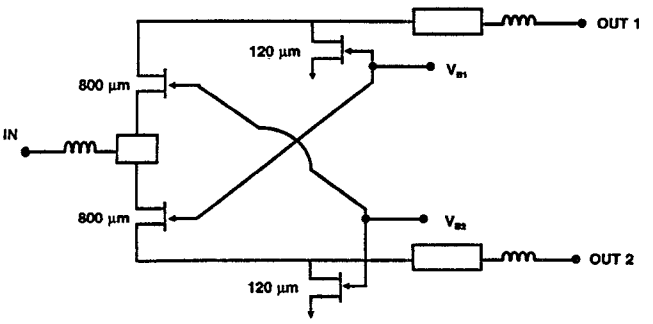

Figure 4. CFET SPDT Switch Schematic

or source-drain contacts, can be spaced as close as the optical lithography will allow. CFETs have been made with source-drain spacing of 1.25 µm. The n-layer is etched outside the device area down to the p-layer. The p-layer is then defined and etched to provide a resistive extension for the CFET gate contact. The resistance of this p-region serves the same function as the gate resistor in a MESFET control element, mainly to isolate the rf from the dc bias line. The p-layer is contacted by the first level metal. This quasi-ohmic contact allows positive bias on the gate with little bias current to be drawn even with 10 volts. After this step the transmission lines, capacitors, and other components of the MMIC are processed by the normal MESFET process.

Performance

Figure 4 shows the schematic for an SPDT switch using a 800-µm series CFET and a 120-µm shunt CFET. The source-drain spacing for the CFET's is 2.5 µm. The chip size is 889 µm by 508 µm. The performance of the CFET SPDT switch from dc to 20 GHz is shown in Figure 5. The insertion loss shown includes the loss of the bond wires. Approximately 0.5 dB of insertion loss at 20 GHz is caused by these bond wires and could be matched out by proper design of the input and output bond pad configuration.

Conclusions

A new high quality control element (CFET) has been demonstrated, which has demonstrated a figure of merit over 800 GHz. The CFET was used in a SPDT switch to demonstrate its state-of-the-art performance. This provides an alternate control element between the relatively lossy MESFET and power consuming PIN diode.

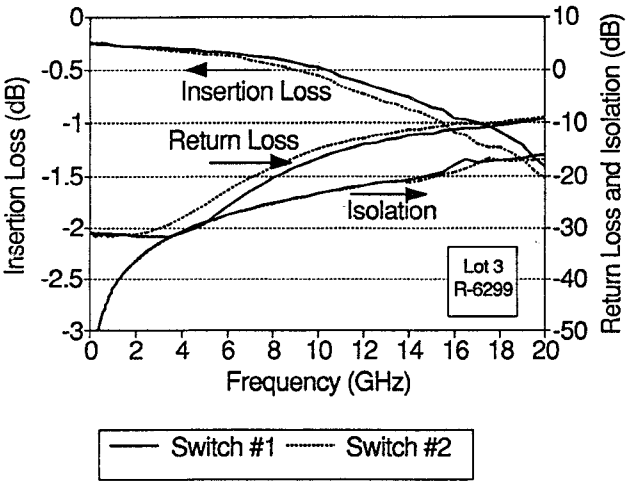

Figure 5. CFET SPDT RF Performance

Acknowledgements

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References

[1] Robert P. Coats, David Seymour, Randy Lehmann and Jeff Helvey, "Wideband Monolithic Phase Shift Realization Using Back-Gate FET Technology"